## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Art Unit:

Not assigned

Takayoshi OBINATA

Examiner: Not assigned

Serial No: Not assigned

Filed: March 15, 2004

For:

Semiconductor Wafer, Semiconductor Device and

Method for Manufacturing Same, Circuit Board, and

Electronic Apparatus

## TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

Mail Stop PATENT APPLICATION Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

The information disclosure statement submitted herewith is being filed concurrently with the subject application [37 C.F.R. § 1.97(b)] and contains no items of information cited in any communication from a foreign patent office in a counterpart foreign application [37 C.F.R. § 1.97(e)(1)].

If it should be determined that for any reason either an insufficient or excessive fee has been paid, please charge any insufficiency or credit any overpayment necessary to ensure consideration of the information disclosure statement for the above-identified application to Deposit Account No. 50-1314. A copy of this paper is enclosed.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

By:

Date: March 15, 2004

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)			Docket Number (Optional) 81754.0110		Application Number Not assigned	
			Applicant Takayoshi OBINATA			
			Filing Date March 15,	Filing Date March 15, 2004		Group Art Unit Not assigned
		U.S. PATEN	T DOCUMENTS			· <del></del>
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
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